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IMPLEMENTATION OF LOW-POWER AND AREA-EFFICIENT 64BIT CARRY SELECT ADDER

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ABSTRACT

Now a day's hottest area of research in VLSI system is design of the area, high-speed and power-efficient data path logic systems. All processor consisting of Arithmetic & logical Unit (ALU) and adder plays an important role for design of ALU. In digital adders, the speed of addition is limited by the time required to send a carry through the adder. Carry Select Adder (CSLA) is an efficient is used for data-processing processors to perform fast arithmetic functions. The proposed work reduces area and power consumption to a great extent with the help of a simple ripple carry adder (RCA) and gate-level architecture. Regular CSLA consist of two RCA and proposed design has been projected by single RCA. This improves the performance of the proposed designs then the regular designs in terms of power consumption and area.

KEYWORDS: *Square Root (SQRT), Application-specific integrated circuit (ASIC), Carry Select Adder area-efficient, CSLA, low power, binary to excess one convertor (BEC).*

INTRODUCTION

The VLSI system design provide us with a huge research in design of area and power-efficient high-speed data path logic system. The digital adders used in Arithmetic & logical Unit (ALU). The speed of addition is depended upon the time required to propagate a carry through the adder.

The addtion of each bit position in an basic adder is generated sequentially only after the previous bit position has been added and a carry propagated into the next position [1].

In the full adder circuit, the carry has to travel from one state to another state. The carry of Last state is required for the present state to perform the operation. Hence, when we increase the number of bits the propagation delay and the delay of each stage increases. by predicting the carry of every stage, we can now avoid the delay occurred in transmitting carry. Now a day our computers speed is upgraded very fast in terms of GHz. So there is a need of improving the speed for the design by developing reduced gate architecture. Carry Select Adder (CSLA) has a more balanced delay and acquires lower power and area [3]. The CSLA is used in many Processors to alleviate the issue of propagation delay by predicting multiple carries independently and then select a carry to generate the sum [2]. As CSLA uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input cin=0 and cin=1, then the final sum and carry are selected by the multiplexers which is considered to be area inefficient.[3]

Ripple carry adder

Ripple Carry Adder consists of cascaded "N" single bit full adders. Output carry of previous adder becomes the input carry of next full adder. Therefore, the carry of this adder traverses longest path called worst case delay path through N stages. Fig.1 shows the block diagram of ripple carry adder. Now as the value of N increases, delay of adder will also increase in a linear way Therefore, RCA has the lowest speed amongst all the adders because of large propagation Delay but it occupies the least area.

Now CSLA provides a way to get around this linear dependency is to anticipate all possible values of input carry i.e. 0 and 1 and evaluate the result in advance. Once the original value of carry is known, result can be selected using the multiplexer stage. Therefore the conventional CSLA makes use of Dual RCA's to generate the partial sum and carry by considering input carry Cin=0 and Cin=1, then the final sum and carry are selected by multiplexers.

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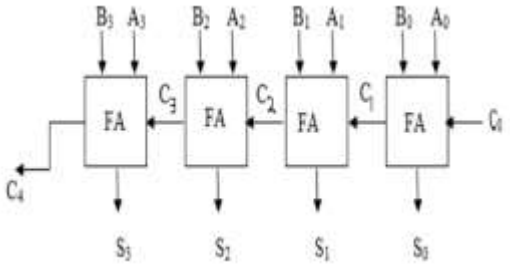

Fig1. 4-bit ripple carry adder

ARCHITECTURE OF REGULAR 64 BIT CSLA

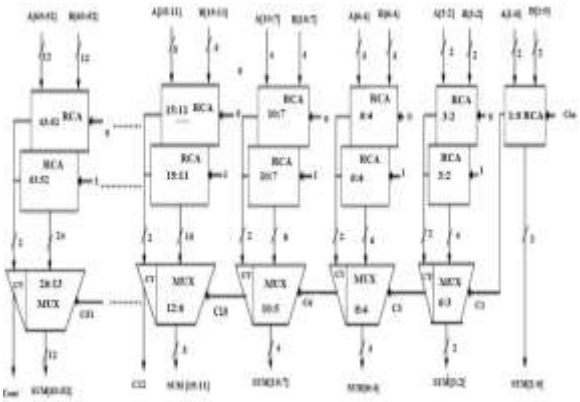

Fig 2: 64-bit CSLA

A carry select adder can be developed in two different sizes namely uniform block size and variable block size. Similarly a 32 and 128-bit can also be developed in two modes of different block sizes. Ripple-carry adders are the simplest and most compact full adders, but their performance is limited by a carry that must propagate from the least-significant bit to the most-significant bit. The various 16, 32, 64 and 128-bit CSLA can also be developed by using ripple carry adders. The speed of a carry-select adder can be improved up to 40% to 90%, by performing the additions in parallel, and reducing the maximum carry delay. Fig shows the Regular structure of 64-bit SQRT CSLA. It includes many ripple carry adders of variable sizes which are divided into groups. Group 0 contains 2-bit RCA which contains only one ripple carry adder which adds the input bits and the input carry and results to sum [1:0] and the carry out. The carry out of the Group 0 which acts as the selection input to mux which is in group 1, selects the result from the corresponding RCA (Cin=0) or RCA (Cin=1). Similarly the remaining groups will be selected depending on the Cout from the previous groups.

BEC:

The basic idea of this work is to achieve lower area and power consumptions with help of Binary to Excess-1 Converter (BEC) instead of using RCA within the regular CSLA [1]. The CSLA needs more area because of using multiples of Ripple Carry Adder for generating sum and carry on the dependency of carry input Cin=0 and Cin=1. Then the final results of sum and carry are selected by the multiplexers from one bit to other going to increase. lastly, results in the output will depend upon number of stages.

BEC is an ADD(+1) circuit which is been used instead of the RCA with C = 1 in order to reduce the area and power consumption of the regular CSLA. To replace n-bit RCA, n+1 bit BEC is required. A structure of a 4-bit BEC is shown in Fig 1.

The basic function of the CSLA is obtained by using the N-bit BEC together with the Mux. One input of the 2N: N Mux gets as it input and N-Bits input of the Multiplexer is the BEC output.

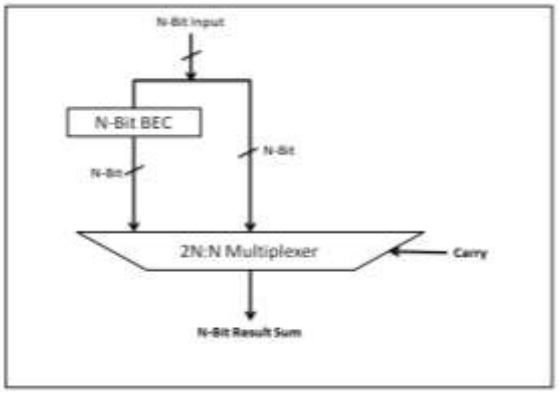

Fig 3: N-bit BEC

This produces the two possible results with carry in parallel and the mux is used to select either the BEC output or the direct inputs according to the control signal Carry from previous stage. The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed [7]. The Boolean expressions as follows.

$$X0 = \overline{B0}$$
$$X1 = B0 \oplus B1$$
$$X2 = B2 \oplus (B0\ B1)$$
$$X3 = B3 \oplus (B0\ B1\ B2)$$

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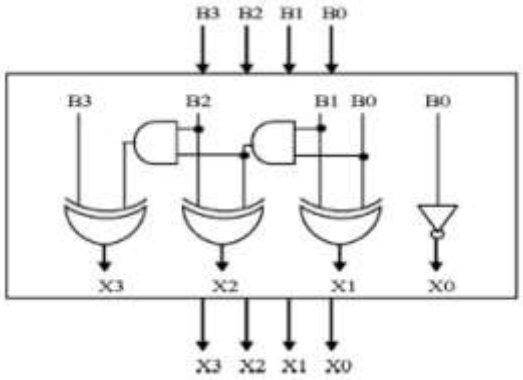

Fig 4. Architecture of 4-bit BEC

Table-1 Input and Output of 4-bit BEC

B[3:0]	X[3:0]
0000	0001
0001	0010
⋮	⋮
1110	1111
1111	0000

Architecture of modified 64-bit SQRT CSLA

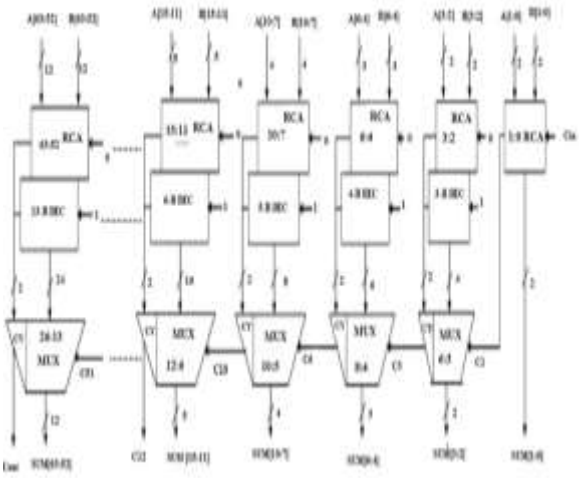

Fig 5: Architecture of modified 64-bit SQRT CSLA

This architecture is similar to regular 64-bit SQRT CSLA, the only change is that, we replace RCA with Cin=1 among the two available RCAs in a group with a BEC. This BEC has a feature that it can perform the similar operation as that of the replaced RCA with Cin=1. Fig 4 shows the Modified block diagram of 64-bit SQRT CSLA. The number of bits required for BEC logic is 1 bit more than the RCA bits. The modified block diagram is also divided into various groups of variable sizes of bits with each group having the ripple carry adders, BEC and corresponding mux. As shown in the Fig.4, Group 0 contain one RCA only which is having input of lower significant bit and carry in bit and produces result of sum [1:0] and carry out which is acting as mux selection line for the next group, similarly the procedure continues for higher groups but they includes BEC logic instead of RCA with Cin=1.Based on the consideration of delay values, the arrival time of selection input C1 of 8:3 mux is earlier than the sum of RCA and BEC. For remaining groups the selection input arrival is later than the RCA and BEC. Thus, the sum1 and c1(output from mux) are depending on mux and results computed by RCA and BEC respectively. The sum2 depends on c1 and mux. For the remaining parts the arrival time of mux selection input is always greater than the arrival time of data inputs from the BEC's. Thus, the delay of the remaining MUX depends on the arrival time of mux selection input and the mux delay. In this Modified CSLA architecture, the implementation code for Full Adder and Multiplexers of 6:3, 8:4, and 10:5 up to 24:11 were designed. The design code for the BEC was designed by using NOT, XOR and AND gates. Then 2, 3, 4, 5 up to 11-bit ripple carry adder was designed.

CONCLUSION

The proposed method reduces the area and power of CSLA architecture. The reduced number of gates in this technique offers the great advantage in the reduction of area and also the total power. The modified CSLA architecture is therefore, low area, low power and efficient for VLSI hardware implementation.

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